What Is Claimed Is:

1. A receiver apparatus for receiving digital data in which stuff data have been inserted by stuffing synchronization, comprising:

a memory unit having a plurality of memory cells to which consecutive addresses are assigned;

a write unit for sequentially designating said addresses in a prescribed order direction and for writing said digital data to the memory cells at the designated addresses, in synchronization with a write clock signal generated on basis of a clock signal synchronized with said digital data;

a write controller for prohibiting said write unit from designating said address at least for said stuff data and from writing at least stuff data;

a read clock signal generator for generating a read clock signal used for reading out digital data stored in said memory unit;

a read unit for sequentially designating said addresses in said memory unit in said prescribed order direction and for reading out digital data stored in memory cells at the designated addresses in synchronization with said read clock signal; and

a read clock signal regulator for adjusting a cycle of said read clock signal based on an interval in said prescribed order direction from an address designated

by said read unit to an address designated by said write unit.

2. The receiver apparatus according to claim 1, wherein said read clock signal regulator performs adjustment of said read clock signals in parts at a plurality of adjustment timings.

3. The receiver apparatus according to claim 1, wherein said read clock signal regulator maintains a current read clock signal cycle when the interval in said prescribed order direction is a predetermined interval, makes a cycle of said read clock signal longer than the current cycle when said interval is shorter than said predetermined interval, and makes a cycle of said read clock signal shorter than the current cycle when said interval is longer than said predetermined interval.

4. The receiver apparatus according to claim 1, wherein said read clock signal regulator holds a first table and a second table, and adjusts the cycle of said read clock signal on basis of said first and second tables, said first table associating the interval in said prescribed order direction and an adjustment amount for said cycle, said second table setting a timing for adjusting said cycle by said adjustment amount in one adjustment, or, alternatively, setting timings for

adjusting said cycle by dividing said adjustment amount into a plurality, and executing a plurality of adjustments each by said divided adjustment amount.

5. The receiver apparatus according to claim 4, wherein intervals between said plurality of timings in said second table are substantially equal time intervals.

6. The receiver apparatus according to claim 4, wherein said read clock signal generator comprises:

a phase-locked loop circuit having as input signals said write clock signal and a signal resulting from dividing its own output signal with a variable frequency divider; and

a frequency divider for dividing an output signal of said phase-locked loop circuit with a division ratio of the same numerical value as the number of bits held in each of said memory cells, and sending the divided signal to said read unit; and wherein

said read clock signal regulator increments or decrements a division ratio of said variable frequency divider by 1 from the division ratio of the same numerical value as the number of said bits, and thereby adjusts the cycle of said read clock signal.

7. The receiver apparatus according to claim 4, wherein said read clock signal generator comprises:

a phase-locked loop circuit; and

a frequency divider having a division ratio of the same numerical value as the number of bits held in each of said memory cells, and for sending a divided signal to said read unit;

said phase-locked loop circuit has as input signals a signal resulting from division by a variable frequency divider of an input clock signal having the same frequency as receiving speed of said digital data, and output signal of said frequency divider; and wherein

said read clock signal regulator increments or decrements a division ratio of said variable frequency divider by 1 from a division ratio of the same numerical value as said number of bits, and thereby adjusts the cycle of said read clock signal.

8. The receiver apparatus according to claim 6, wherein said digital data are received in units of frames having a payload part and an overhead part; said payload part having communication data to be written to said memory unit and, when positive stuffing is effected, said stuff data; said overhead part having control data and, when negative stuffing is effected, communication data that should be contained in said payload part;

said write controller prohibits said write unit from said address designation and from writing data, for

the stuff data in the payload part and all those data other than the communication data in said overhead part;

said phase-locked loop comprises:

a first frequency divider for dividing said write clock signal with a division ratio of N;

a second frequency divider for dividing an output signal of said variable frequency divider with a division ratio of M;

a phase comparator for finding phase difference between output signals of said first frequency divider and said second frequency divider;

a low-pass filter for filtering an output signal of said phase comparator; and

a voltage control oscillator to which is input signal filtered by said low-pass filter; and

said N and M are any numerical values with which N : M becomes equivalent to the ratio between data volume of said overhead part and data volume of said payload part.

9. The receiver apparatus according to claim 7, wherein said digital data are received in units of frames having a payload part and an overhead part; said payload part having communication data to be written to said memory unit and, when positive stuffing is effected, said stuff data; said overhead part having control data and, when negative stuffing is effected, communication data that should be contained in said payload part;

said write controller prohibits said write unit from designating said address and from writing data, for the stuff data in the payload part and all those data other than the communication data in said overhead part;

said phase-locked loop comprises:

a first frequency divider for dividing said write clock signal with a division ratio of N;

a second frequency divider for dividing an output signal of said variable frequency divider with a division ratio of M;

a phase comparator for finding phase difference between output signals of said first frequency divider and said second frequency divider;

a low-pass filter for filtering an output signal of said phase comparator; and

a voltage control oscillator to which is input signal filtered by said low-pass filter; and

said N and M are any numerical values with which N : M becomes equivalent to a ratio between data volume of said overhead part and data volume of said payload part.

10. The receiver apparatus according to claim 4, wherein said digital data are received in units of frames having a payload part and an overhead part; said payload part having communication data to be written to said memory unit and, when positive stuffing is effected, said stuff data; said overhead part having control data and, when

negative stuffing is effected, communication data that should be contained in said payload part;

said write controller prohibits said write unit from designating said address and from writing data, for the stuff data in the payload part and all those data other than the communication data in said overhead part;

said read clock signal generator comprises:

a voltage control oscillator;

a first frequency divider for dividing an input clock signal having the same frequency as said digital data with a division ratio of N;

a second frequency divider for dividing an output signal of said voltage control oscillator with a division ratio of M or a division ratio of M±1;

a phase comparator for finding phase difference between output signals of said first frequency divider and said second frequency divider;

a low-pass filter for filtering an output signal of said phase comparator and sending a filtered signal to said voltage control oscillator; and

a third frequency divider for dividing the output signal of said voltage control oscillator with a division ratio of the same numerical value as the number of bits held in each of the memory cells, and sending a divided signal as said read clock signal to said read unit;

said N and M are any numerical values with which N:M becomes equivalent to a ratio between data volume of

said overhead part and data volume of said payload part; and

said read clock signal regulator increments or decrements the division ratio of said second frequency divider by 1 from said M, and thereby changes the cycle of said read clock signal.

11. The receiver apparatus according to claim 4, wherein said digital data are received in units of frames having a payload part and an overhead part; said payload part having communication data to be written to said memory unit and, when positive stuffing is effected, said stuff data; said overhead part having control data and, when negative stuffing is effected, communication data that should be contained in said payload part;

said write controller prohibits said write unit from designating said address and from writing data, for the stuff data in the payload part and all those data other than the communication data in the overhead part;

said read clock signal generator comprises:

a voltage control oscillator;

a first frequency divider for dividing an input clock signal having the same frequency as said digital data with a division ratio of N or a division ratio of N±1;

a second frequency divider for dividing an output signal of said voltage control oscillator with a division ratio of M;

a phase comparator for finding phase difference between output signals of said first frequency divider and said second frequency divider;

a low-pass filter for filtering an output signal of said phase comparator and sending a filtered signal to said voltage control oscillator; and

a third frequency divider for dividing the output signal of said voltage control oscillator with a division ratio of the same numerical value as the number of bits held in each of the memory cells, and sending a divided signal as said read clock signal to said read unit;

said N and M are any numerical values wherewith N:M becomes equivalent to a ratio between data volume of said overhead part and data volume of said payload part; and

said read clock signal regulator increments or decrements the division ratio of said first frequency divider by 1 from said N, and thereby changes the cycle of said read clock signal.